

Case No.: AMKOR-017A (SK-017A)

SEMICONDUCTOR PACKAGE WITH STACKED DIES

INVENTOR

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CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims priority to Korean Patent Application No. 2001-02163 entitled SEMICONDUCTOR PACKAGE filed January 15, 2001.

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT  
(Not Applicable)

BACKGROUND OF THE INVENTION

**1. Field of the Invention**

[0001] The present invention relates generally to semiconductor packages, and more particularly to a semiconductor package which includes a stacked pair of semiconductor dies, one of which is electrically connected to the leads of the semiconductor package in a manner facilitating a reduction in the size of the semiconductor package.

**2. Description of the Related Art**

[0002] As is well known in the electrical arts, recent advances in semiconductor package technology have led to the development of packaging techniques which provide for the continuing miniaturization of the semiconductor package. These advancements have also led to the

development of a wide variety of new and differing types of semiconductor packages. Consistently in high demand are those semiconductor packages which have a high capacity and are capable of performing various functions. However, those currently known semiconductor packages including only a single semiconductor die are limited in their ability to perform multi-functions. To address this limitation, there has been developed in the prior art various semiconductor packages in which semiconductor dies or the semiconductor packages themselves are stacked on each other. However, these semiconductor packages have structural limits attributable to the stacking of the dies or packages therein, and are often of a size which decreases or diminishes their utility in certain applications. The present invention is specifically adapted to address this deficiency, as will be discussed in more detail below.

#### BRIEF SUMMARY OF THE INVENTION

**[0003]** In accordance with the present invention, there is provided a semiconductor package which comprises a plurality of leads. Each of the leads defines opposed first and second surfaces, and a third surface which is also disposed in opposed relation to the second surface. The first surface is oriented between the second and third surfaces. Also included in the semiconductor package are first and second semiconductor dies which each define opposed first and second surfaces. A plurality of bond pads are disposed on the first surface of the first semiconductor die, with bond pads also being disposed on the second surface of the second semiconductor die. The first surface of the first semiconductor die is attached to the second surface of each of the leads, with the first surface of the second semiconductor die being attached to

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the second surface of the first semiconductor die.

**[0004]** In the semiconductor package, a plurality of conductive wires are used to electrically connect the bond pads of the first semiconductor die to respective ones of the first surfaces of the leads. Conductive wires are also used to electrically connect the bond pads of the second semiconductor die to respective ones of the second surfaces of the leads. An encapsulating portion is applied to the leads, the first and second semiconductor dies, and the conductive wires, with the third surface of each of the leads being exposed within the encapsulating portion.

**[0005]** In the semiconductor package of the present invention, the first semiconductor die and the leads are oriented relative to each other such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads. As such, the bond pads of the first semiconductor die do not contact the second surface of any one of the leads. The conductive wires electrically connecting the bond pads of the first semiconductor die to the leads are thus oriented inwardly relative to the peripheral edge of the first semiconductor die. This relative orientation facilitates a reduction in the size of the semiconductor package.

**[0006]** The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0007]** These, as well as other features of the present invention, will become more apparent upon reference to the drawings wherein:

**[0008]** Figure 1 is a cross-sectional view of a semiconductor package constructed in accordance with the

present invention;

[0009] Figure 1A is a bottom plan view of the semiconductor package shown in Figure 1, excluding the encapsulating portion thereof;

[0010] Figure 1B is a top plan view of the semiconductor package shown in Figure 1, excluding the encapsulating portion thereof; and

[0011] Figures 2A through 2E are cross-sectional views illustrating a sequence of steps which may be employed for manufacturing the semiconductor package of the present invention.

[0012] Common reference numerals are used throughout the drawings and detailed description to indicate like elements.

#### DETAILED DESCRIPTION OF THE INVENTION

[0013] Referring now to the drawings wherein the showings are for purposes of illustrating a preferred embodiment of the present invention only, and not for purposes of limiting the same, Figure 1 provides a cross-sectional view of a semiconductor package 100 constructed in accordance with the present invention. The semiconductor package 100 comprises a plurality of identically configured leads 130. Each of the leads 130 defines a generally planar first (lower) surface 131a and a generally planar second (upper) surface 131b which is disposed in opposed relation to the first surface 131a. Each lead 130 further defines a generally planar third (lower) surface 131c which is also disposed in opposed relation to the second surface 131b and is laterally offset outwardly relative to the first surface 131a. More particularly, the thickness between the second and third surfaces 131b, 131c exceeds the thickness between the first and second surfaces 131a, 131b. The first surfaces 131a of

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the leads 130 are each preferably formed by a conventional half etching technique using chemical solutions.

**[0014]** In addition to the leads 130, the semiconductor package 100 includes a die paddle 135 which is of a predetermined thickness. The preferred thickness of the die paddle 135 is preferably the same as the thickness between the second and third surfaces 131b, 131c of each of the leads 130. The leads 130 and die paddle 135 are oriented relative to each other such that the leads 130 are arranged about the periphery of the die paddle 135 in the manner best shown in Figure 1A. The die paddle 135 has a generally square configuration, with the leads 130 being segregated into four sets of four, and each set extending along a respective one of the four peripheral edge segments defined by the die paddle 135. As seen in Figures 1 and 1A, the innermost end of each lead 130 is disposed in spaced relation to the corresponding peripheral edge segment of the die paddle 135. Those of ordinary skill in the art will recognize that differing numbers of leads 130 in differing arrangements may be included in the semiconductor package 100, with the size, shape and arrangement of the leads 130 and die paddle 135 as shown in Figures 1, 1A and 1B being for exemplary purposes only.

**[0015]** The semiconductor package 100 of the present invention further comprises a first semiconductor die 110 which defines a first surface 111a and a second surface 111b which is disposed in opposed relation to the first surface 111a. The first semiconductor die 110 further includes a plurality of bond pads 113 which are disposed on the first surface 111a thereof. In the semiconductor package 100, portions of the first surface 111a of the first semiconductor die 110 are bonded to the second surface 131b of each lead 130 and to the top surface of the die paddle 135 through the use of a layer of a die attach

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material 160. The die attach material 160 may be any one of a non-conductive epoxy, a non-conductive polyimide, a non-conductive double-faced adhesive tape or its equivalent, with the present invention not being limited by any particular die attach material 160.

**[0016]** In addition to the first semiconductor die 110, the semiconductor package 100 includes a second semiconductor die 120. The second semiconductor die 120 defines a first surface 121a and a second surface 121b which is disposed in opposed relation to the first surface 121a. Disposed on the second surface 121b are a plurality of bond pads 123. The first surface 121a of the second semiconductor die 120 is bonded to the second surface 111b of the first semiconductor die 110 by another layer of the die attach material 160.

**[0017]** As seen in Figure 1A, the first semiconductor die 110 and leads 130 are arranged relative to each other such that the bond pads 113 of the first semiconductor die 110 are each oriented between a respective pair of the leads 130 when the first surface 111a of the first semiconductor die 110 is bonded to the second surfaces 131b of the leads 130. In this regard, it is important in the semiconductor package 100 that none of the bond pads 113 contact any of the second surfaces 131b of the leads 130 when the first surface 111a of the semiconductor die 110 is bonded to the second surfaces 131b of the leads 130. In the semiconductor package 100, each bond pad 113 of the first semiconductor die 120 is electrically connected to the first surface 131a of a respective one of the leads 130 by a first conductive connector 151 such as a conductive wire. Similarly, as seen in Figures 1 and 1B, each bond pad 123 of the second semiconductor die 120 is electrically connected to the second surface 131b of a respective one of the leads 130 by a second conductive connector 153 such as

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a conductive wire. The conductive connectors 151, 153 may each be any one of a gold wire, an aluminum wire, or its equivalent, with the present invention not being limited by any particular material for the conductive connectors 151, 153.

**[0018]** As indicated above, the bond pads 113 of the first semiconductor die 110 are each located between a respective pair of leads 130. Thus, the electrical connection between the bond pads 113 and the first surfaces 131a of the leads 130 through the use of the conductive connectors 151 can be accomplished in a manner wherein the conductive connectors 151 are each located inwardly relative to the peripheral edge of the first semiconductor die 110. As seen in Figure 1, the peripheral edge of the first semiconductor die 110 extends to approximately that portion of the second surface 131b of each lead 130 which is disposed in opposed relation to the third surface 131c.

**[0019]** In the semiconductor package 100, the first and second semiconductor dies 110, 120, the leads 130, and the conductive connectors 151, 153 are each encapsulated by an encapsulant in order to protect the same from the external environment. The hardening of the encapsulant defines an encapsulating portion 180 of the semiconductor package 100. The encapsulating portion 180 is formed such that the third surface 131c of each of the leads 130 and the bottom surface of the die paddle 135 are exposed within the encapsulating portion 180, and in particular the bottom surface defined thereby. Also exposed in the side surfaces of the encapsulating portion 180 is the outermost end of each of the leads 130. The exposed third surfaces 131c of the leads 130 may be electrically connected to an external device (e.g., a motherboard). Additionally, the exposed third surfaces 131c of the leads 130 and bottom surface of the die paddle 135 within the encapsulating portion 180

function as heat sinks which allow for the emission of heat generated by the first and second semiconductor dies 110, 120.

**[0020]** It is contemplated that the first and second semiconductor dies 110, 120 will have identical functions since the semiconductor dies 110, 120 are electrically connected to common leads 130. However, it is also contemplated that the first and second semiconductor dies 110, 120 may have different functions. In this case, the first semiconductor die 110 would be electrically connected to the first surfaces 131a of certain ones of the leads 130, with the second semiconductor die 120 being electrically connected to the second surfaces 131b of certain ones of the leads 130 which are not electrically connected to the first semiconductor die 110. As such, the first and second semiconductor dies 110, 120 would not be electrically connected to any common lead 130. The orientation of the conductive connectors 151 inwardly of the peripheral edges of the stacked semiconductor dies 110, 120 allows for a reduction in the size of the semiconductor package 100.

**[0021]** Referring now to Figures 2A through 2E, the manufacturing method for the semiconductor package 100 of the present invention preferably comprises the initial step of providing the leads 130 and die paddle 135 oriented relative to each other in the above-described manner. Thereafter, the first surface 111a of the first semiconductor die 110 is bonded to the second surface 131b of each of the leads 130 and to the top surface of the die paddle 135 through the use of the die attach material 160 in the above-described manner (Figure 2A). As explained above, the first semiconductor die 110 and the leads 130 are oriented relative to each other such that the bond pads 113 of the first semiconductor die 110 are not in direct

contact with any of the second surfaces 131b of the leads 130, but rather are each oriented between a respective pair of the leads 130.

**[0022]** Subsequent to the attachment of the first semiconductor die 110 to the leads 130 and die paddle 135, the bond pads 113 of the first semiconductor die 110 are electrically connected to respective ones of the first surfaces 131a of the leads 130 through the use of the first conductive connectors 151 (Figure 2B). Thereafter, the first surface 121a of the second semiconductor die 120 is bonded to the second surface 111b of the first semiconductor die 110 by another layer of the die attach material 160 (Figure 2C).

**[0023]** Subsequent to the attachment of the second semiconductor die 120 to the first semiconductor die 110, the bond pads 123 of the second semiconductor die 120 are electrically connected to respective ones of the second surfaces 131b of the leads 130 through the use of the second conductive connectors 153 in the above-described manner (Figure 2D). Thereafter, the encapsulant is applied to the first and second semiconductor dies 110, 120, the leads 130 and the first and second conductive connectors 151, 153 to encapsulate the same and form the encapsulating portion 180 (Figure 2E). As indicated above, the encapsulating portion 180 protects the first and second semiconductor dies 110, 120, the leads 130, and the first and second conductive connectors 151, 153 from the external environment.

**[0024]** It is contemplated that the second semiconductor die 120 may be bonded to the first semiconductor die 110 via a layer of the die attach material 160, with the first semiconductor die 110 thereafter being bonded to the leads 130 in the above-described manner. It is further contemplated that the bonding order of the first and second

conductive connectors 151, 153 used to facilitate the electrical connection of the first and second semiconductor dies 110, 120, respectively, to the leads 130 can be changed or reversed from that described above if warranted by the circumstance.

**[0025]** This disclosure provides exemplary embodiments of the present invention. The scope of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for by the specification or implied by the specification, such as variations in structure, dimension, type of material or manufacturing process may be implemented by one of skill in the art in view of this disclosure.